HIO-EMB-1200

Technical Specification Manual

Version: R1.00

Revisions

Version	Description of Version	Date Completed
D0.01	Draft	2014/10/30
R1.00	Initial Release	2015/06/06

Preface

This Technical Specification Manual (TSM) specifies the board layout, components, connectors, and the I/O connection ports, motherboards features.

Intended Audience

The TSM is intended to provide detailed, technical information about the HIO-EMB-1200 and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

What This Document Contains

Chapter	Description
1	Introduction
2	Product Description
3	Technical Reference
4	Operating System

1. Introduction

1.1 Product introduction

The HIO-EMB-1200 is ultra small form factor embedded board based on Freescale i.MX6 Cortex A9 ARM platform. It has a Freescale i.MX6DL or i.MX6Q on board with on board DDR3 memory and iNAND flash storage. The I/O interfaces include: HDMI, USB2.0, micro SD slot, serial console, OTG and 200 pin headers on the top and bottom to bring out all the display ports, camera ports, CAN, serial, I2C, SPI, SDIO and more i.MX6 I/O resources.

1.2 HIoTX Form Factor

The HIoTX form factor is developed for the HIO Project open architecture platform. Measuring just 72mm x 80mm, the HIoTX mainboard is a fully functional ARM computer board with on-board processor, RAM, iNAND flash, HDMI, USB and power input from mainboard or add-on boards. It is 80% smaller than the mini-ITX form factor and 20% smaller than the tiny PICO-ITX standard. The HIoTX form factor leverages the Freescale i.MX application processor's rich I/O and flexibility. The unique modular design of the HIoTX form factor allows 3-dimensional expansion utilizing its 200-pin female header on the top and bottom of the board. The HIoTX form factor is designed to enable rapid prototyping, quick application module development and fast time to market.

2. Product Description

2.1 Specification

Table 1 summarizes the major features of the board.

Table 1. Specification

Essentials	
Platform	Freecasle i.MX6
Form Factor	HIoTX
Processor	Freescale i.MX6DL (default) or i.MX6Q at 1GHz
Core	Cortex-A9 Dual core (i.MX6DL) or Cortex-A9 Quad core (i.MX6Q)
System Memory	64-bit 1GB DDR3 SDRAM 400MHz(i.MX6DL) or 528MHz(i.MX6Q)
Ethernet	Onboard Gigabit Ethernet PHY
Storage	4GB iNand Flash,up to 32GB
Graphic	
Graphic Controller	Vivante GC 880 + Vivante GC 320 (i.MX6DL) Vivante GC 2000 + Vivante GC 355 + Vivante GC 320 (i.MX6Q)
Display Interface	1x mini HDMI
Display Resolution	HDMI - 1920 x 1080
I/O	
SD Card Socket	1 x micro SD Socket (not support hot plug)
USB	2 x 4-pin 2.0 mm pitch USB 2.0 pin headers
Boot Switch	1 x 2-bit DIP switch for iNAND and micro SD boot selection
Power Switch	1 x on-board power switch
Console Port	1 x 4-pin TTL serial port
Power Input	1 x 5V/2A DC power input, 2.5mm OD, 0.7mm ID
OTG	1 x OTG
Expansion	4x 50pin 1.27mm pitch top and bottom I/O expansion. 200-pin top and bottom female headers offers: 24bit Parallel Display Port, dual channel 24bit LVDS, MIPI DSI up to 24bit, MIPI CSI up to 4 lane, 8bit parallel camera interface, GbE PHY, x1 PCIe PHY, 2x USB2.0, I2S audio codec output with Line-out/detect, Line-out, Mic-in/detect, speaker out (1W), 4bit SDIO, IOMUX outputs: up to 5x UART, 2x CAN, 3x SPI, 3x I2C, 34 configurable GPIO
Mechanical & Environmental	
Operating Temperature	-10 ~ 50° C (14 ~ 122° F)
Storage Temperature	-40 ~ 85° C (-40 ~ 185° F)
Operating Humidity	5% ~ 95%, 40ºC, non-condensing
Dimensions	85 x 72 mm (3.34" x 2.84")

2.2 Board Layout

Figure 1 shows the location of the major components on the top and bottom-side of the HIO-EMB-1200.

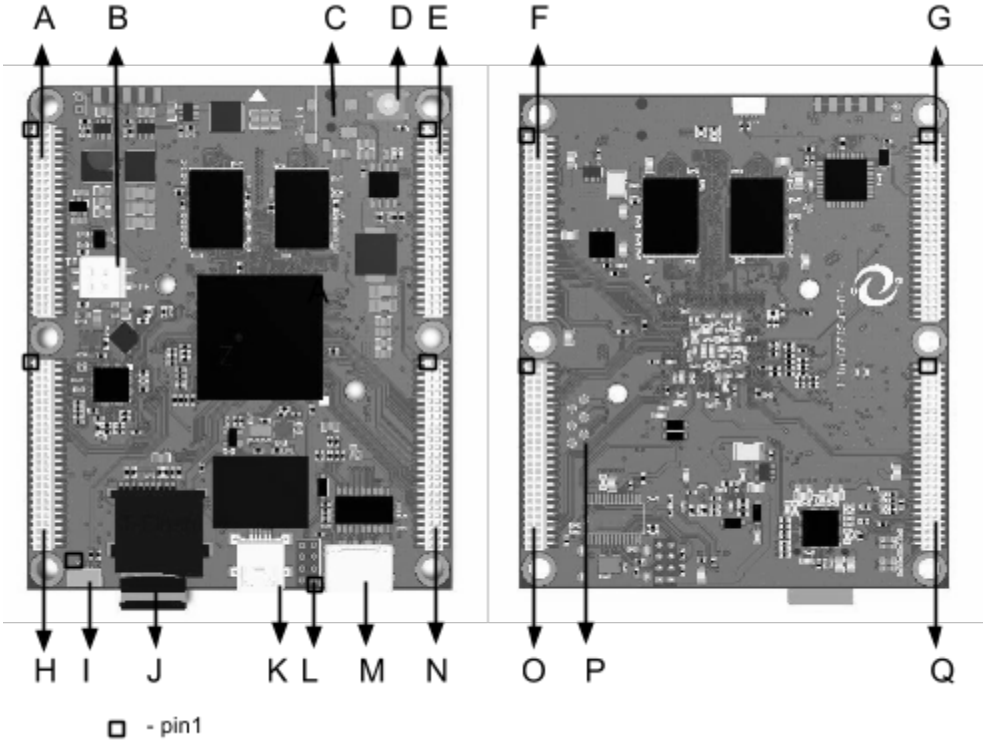


Table 2 lists the components identified in Figure 1

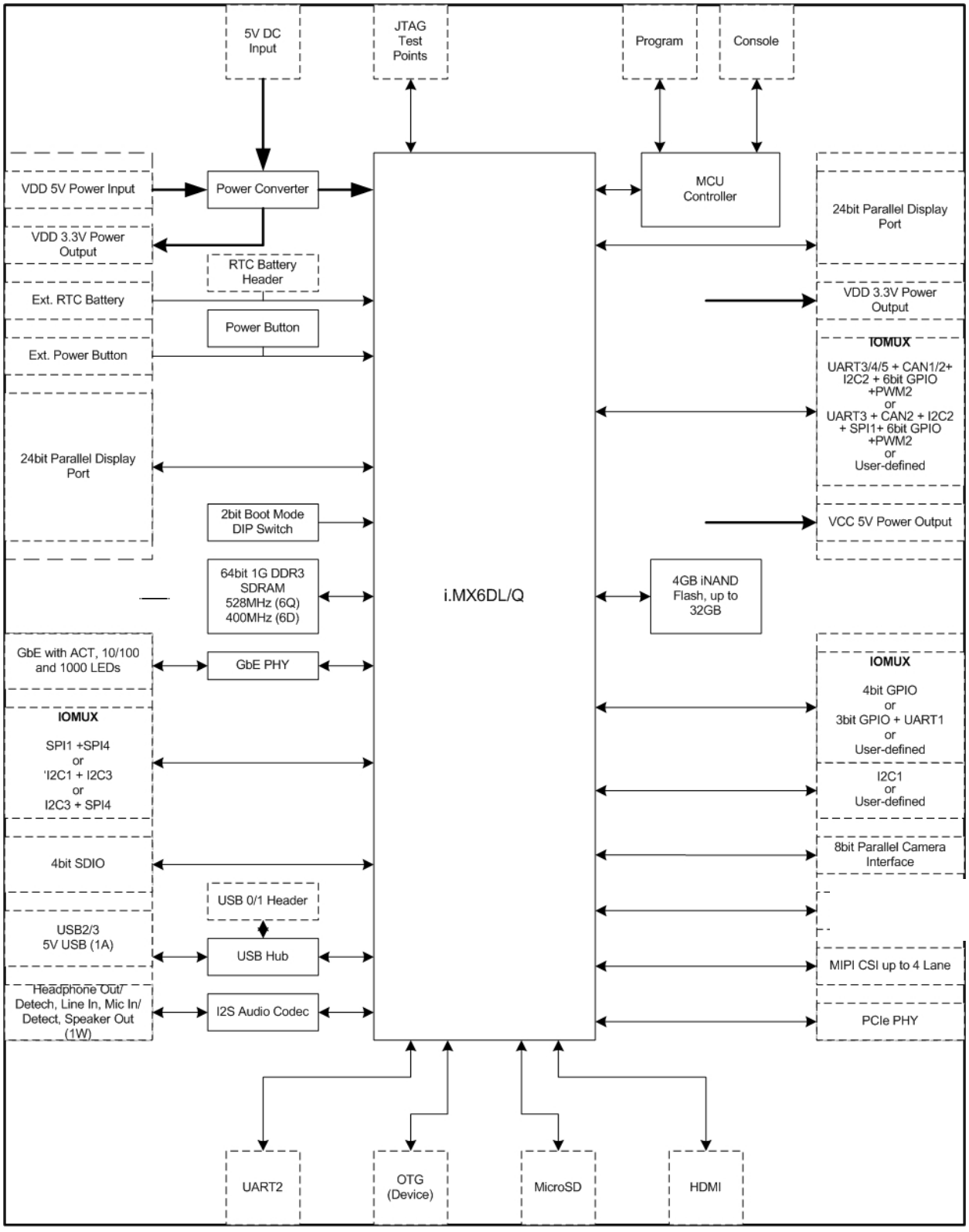
Table 2. Components Show in Figure 1

Item from Figure 1	Connector	Description
A	J606 (Top of J600)	Power, RTC and 24bit parallel display port
B	DIP Switch	2-bit DIP switch for boot selection TF/iNAND
C	DC Jack	5V DC Jack
D	Power Button	
E	J608 (Top of J602)	LVDS, UARTs, CAN, I2C, GPIOs, VDD, VCC
F	J602 (Bottom of J608)	LVDS, UARTs, CAN, I2C, GPIOs, VDD, VCC
G	J600 (Bottom of J606)	Power and 24bit parallel display port
H	J607 (Top of J601)	Audio, USB, SDIO, Ethernet, I2C and SPI
I	Console UART	TTL serial port
J	SD Card Socket	micro SD socket
K	OTG	OTG Device only
L	USB	2x USB 2.0 headers
M	mini HDMI	HDMI with audio
N	J609 (Top of J603)	GPIO, I2C, PCIe PH, MIPI DSI, CSI, Camera
O	J603 (Bottom of J609)	GPIO, I2C, PCIe PH, MIPI DSI, CSI, Camera
P	JTAG	
Q	J601 (Botom of J607)	Audio, USB, SDIO, Ethernet, I2C and SPI

2.3 Block Diagram

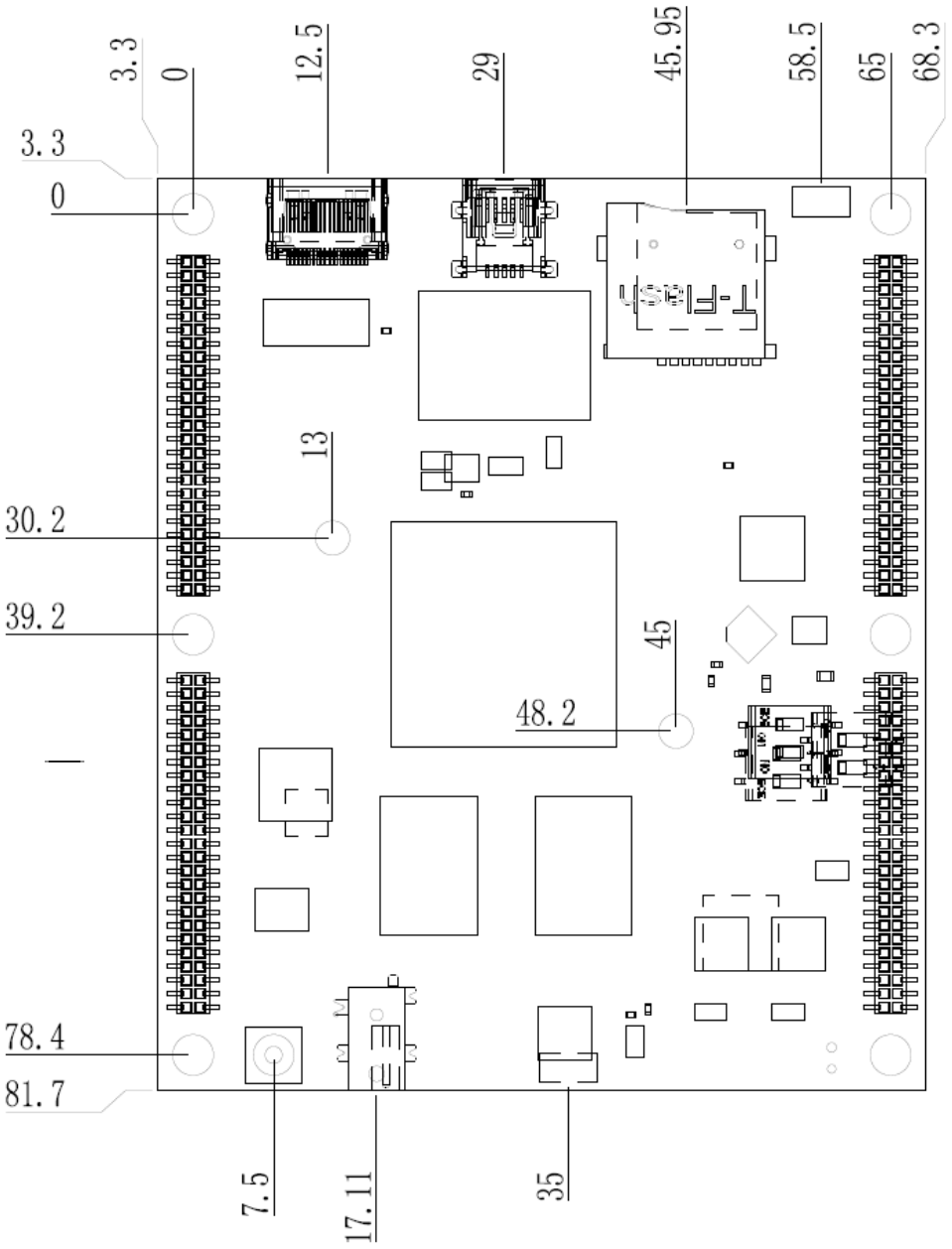
Figure 4 is a block diagram of the major functional areas of the board.

Figure 4. Block Diagram



2.4 Dimensions

Figure 5 is board layout dimensions (unit: mm).



3. Technical Reference

3.1 Connectors and Headers

Table 4. J606 Header (Figure. 1. A)

Pin	Signal Name	Pin	Signal Name
1	GND	26	DISP0_G3
2	GND	27	DISP0_B6
3	GND	28	DISP0_R5
4	GND	29	DISP0_B1
5	VDD_5V	30	DISP0_B3
6	VDD_5V	31	GND
7	VDD_5V	32	DISP0_B2
8	VDD_5V	33	DISP0_G5
9	GND	34	DISP0_G2
10	GND	35	DISP0_VSYNC
11	VDD_3P3V	36	DISP0_B4
12	VDD_3P3V	37	DISP0_B0
13	EXT_PWREN_nBTN	38	DISP0_DE
14	VDD_3P3V	39	GND
15	GND	40	DI0_PIN4
16	VDD_RTC_BAT	41	GND
17	VDD_AO_3P3V	42	DISP0_PCLK
18	GND	43	DISP0_HSYNC
19	DISP0_R2	44	DISP0_B7
20	DISP0_R7	45	DISP0_G4
21	DISP0_R4	46	DISP0_B5
22	DISP0_R3	47	DISP0_R1
23	DISP0_G7	48	DISP0_G1
24	DISP0_R0	49	DISP0_R6
25	DISP0_G0	50	DISP0_G6

Table 5. DIP Switch (Figure. 1. B)

Bit 1	Bit 2	Description
OFF	ON	Boot from micro SD Card
ON	OFF	Boot from iNAND
ON	OFF	No Boot
OFF	OFF	No Boot

Table 6. J608 Header (Figure. 1. E)

Pin	Signal Name	Pin	Signal Name
1	GND	26	LVDS_ODD_0M
2	GND	27	VDD_3P3V
3	LVDS_EVEN_3P	28	KEY_COL0

4	LVDS_EVEN_CLKP	29	KEY_COL2
5	LVDS_EVEN_3M	30	KEY_ROW2
6	LVDS_EVEN_CLKM	31	KEY_ROW0
7	LVDS_EVEN_2P	32	KEY_ROW1
8	LVDS_EVEN_1P	33	KEY_COL1
9	LVDS_EVEN_2M	34	GPIO_6
10	LVDS_EVEN_1M	35	I2C2_SDA
11	GND	36	KEY_COL4
12	GND	37	GPIO_3
13	LVDS_EVEN_0P	38	GPIO_4
14	LVDS_ODD_3P	39	GPIO_7
15	LVDS_EVEN_0M	40	GPIO_5
16	LVDS_ODD_3M	41	GPIO_1
17	LVDS_ODD_CLKP	42	KEY_ROW4
18	LVDS_ODD_2P	43	GPIO_9
19	LVDS_ODD_CLKM	44	I2C2_SCL
20	LVDS_ODD_2M	45	EIM_D25
21	GND	46	EIM_D24
22	GND	47	GND
23	LVDS_ODD_1P	48	GND
24	LVDS_ODD_0P	49	VCC_5V
25	LVDS_ODD_1M	50	VCC_5V

Table 7. J602 Header (Figure. 1. F)

Pin	Signal Name	Pin	Signal Name
1	GND	26	LVDS_ODD_1M
2	GND	27	KEY_COL0
3	LVDS_EVEN_CLKP	28	VDD_3P3V
4	LVDS_EVEN_3P	29	KEY_ROW2
5	LVDS_EVEN_CLKM	30	KEY_COL2
6	LVDS_EVEN_3M	31	KEY_ROW1
7	LVDS_EVEN_1P	32	KEY_ROW0
8	LVDS_EVEN_2P	33	GPIO_6
9	LVDS_EVEN_1M	34	KEY_COL1
10	LVDS_EVEN_2M	35	KEY_COL4
11	GND	36	I2C2_SDA
12	GND	37	GPIO_4
13	LVDS_ODD_3P	38	GPIO_3
14	LVDS_EVEN_0P	39	GPIO_5
15	LVDS_ODD_3M	40	GPIO_7
16	LVDS_EVEN_0M	41	KEY_ROW4
17	LVDS_ODD_2P	42	GPIO_1
18	LVDS_ODD_CLKP	43	I2C2_SCL
19	LVDS_ODD_2M	44	GPIO_9
20	LVDS_ODD_CLKM	45	EIM_D24
21	GND	46	EIM_D25

22	GND	47	GND
23	LVDS_ODD_0P	48	GND
24	LVDS_ODD_1P	49	VCC_5V
25	LVDS_ODD_0M	50	VCC_5V

Table 8. J600 Header (Figure. 1. G)

Pin	Signal Name	Pin	Signal Name
1	GND	26	DISP0_G0
2	GND	27	DISP0_R5
3	GND	28	DISP0_B6
4	GND	29	DISP0_B3
5	VDD_5V	30	DISP0_B1
6	VDD_5V	31	DISP0_B2
7	VDD_5V	32	GND
8	VDD_5V	33	DISP0_G2
9	GND	34	DISP0_G5
10	GND	35	DISP0_B4
11	VDD_3P3V	36	DISP0_VSYNC
12	VDD_3P3V	37	DISP0_DE
13	VDD_3P3V	38	DISP0_B0
14	EXT_PWREN_nBTN	39	DI0_PIN4
15	VDD_RTC_BAT	40	GND
16	GND	41	DISP0_PCLK
17	GND	42	GND
18	VDD_AO_3P3V	43	DISP0_B7
19	DISP0_R7	44	DISP0_HSYNC
20	DISP0_R2	45	DISP0_B5
21	DISP0_R3	46	DISP0_G4
22	DISP0_R4	47	DISP0_G1
23	DISP0_R0	48	DISP0_R1
24	DISP0_G7	49	DISP0_G6
25	DISP0_G3	50	DISP0_R6

Table 10. J607 Header (Figure. 1. H)

Pin	Signal Name	Pin	Signal Name
1	TRXP1	26	SD1_CMD
2	TRXP0	27	SD1_DAT1
3	TRXN1	28	SD1_DAT0
4	TRXN0	29	SD1_DAT3
5	GND	30	SD1_DAT2
6	GND	31	GND
7	TRXP3	32	USB_5V
8	TRXP2	33	USB_HUB_DM2
9	TRXN3	34	USB_HUB_DM1
10	TRXN2	35	USB_HUB_DP2

11	RGMII_LED_1000	36	USB_HUB_DP1
12	RGMII_LED_ACT	37	HP_nINSERT
13	EIM_D17	38	HPO_R
14	RGMII_LED_10_100	39	HPO_GND
15	EIM_D19	40	HPO_L
16	EIM_D18	41	MIC_GND
17	EIM_D28	42	MIC1_N
18	EIM_D16	43	MIC_nDET_GPIO_16
19	EIM_A25	44	LINEIN_R
20	EIM_D22	45	LIN_GND
21	EIM_D21	46	LINEIN_L
22	EIM_D20	47	SPK_LP
23	GND	48	SPK_LN
24	GND	49	SPK_RP
25	SD1_CLK	50	SPK_RN

Table 11. UART Console Port (Figure. 1. l)

Pin	Signal Name
1	GND
2	NC
3	UART2_RXD
4	UART2_TXD

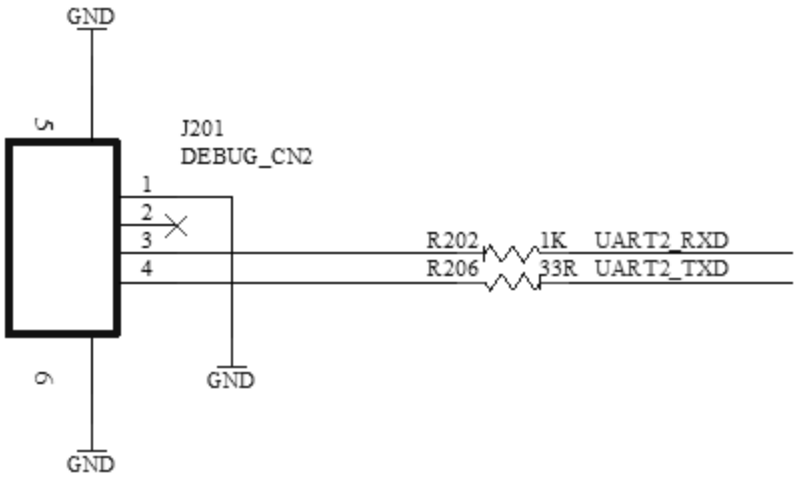


Table 12. OTG Port (Figure. 1.K)

Pin	Signal Name
1	VDD_OTG_VBUS
2	USB_OTG_DM
3	USB_OTG_DP
4	USB_OTG_ID

5	GND

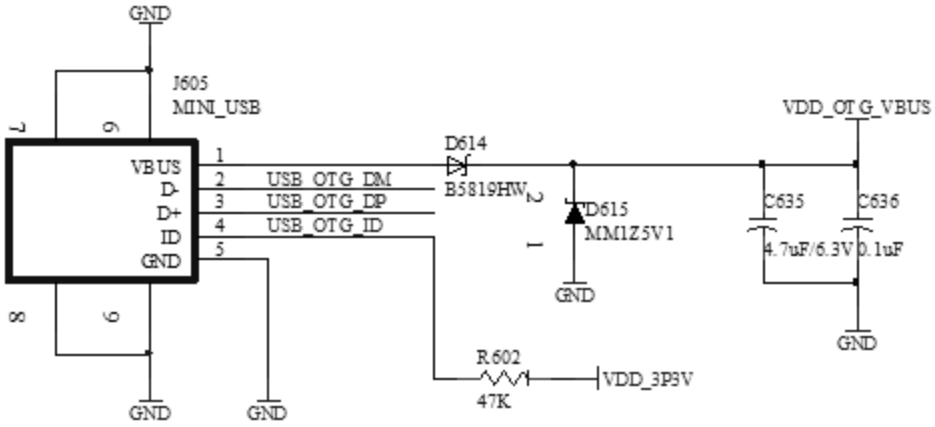


Table 13. USB Header (Figure. 1. L)

Pin	Signal Name
1	USB_5V
3	USB_HUB_DM4
5	USB_HUB_DP4
7	GND
2	USB_5V
4	USB_HUB_DM3
6	USB_HUB_DP3
8	GND

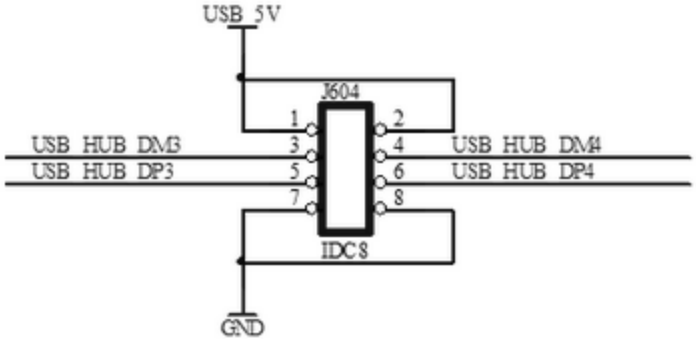


Table 14. HDMI Port (Figure. 1. M)

Pin	Signal Name
1	GND
2	HDMI_D2P
3	HDMI_D2M
4	GND
5	HDMI_D1P

6	HDMI_D1M
7	GND
8	HDMI_D0P
9	HDMI_D0M
10	GND
11	HDMI_CLKP
12	HDMI_CLKM
13	GND
14	HDMI_CEC_OUT
15	HDMI_DDC_CLK_OUT
16	HDMI_DDC_DAT_OUT
17	NC
18	HDMI_5V
19	HPD_OUT

Table 15. J609 Header (Figure. 1. N)

Pin	Signal Name	Pin	Signal Name
1	GPIO_8	26	DSI_D0P
2	GPIO_3	27	DSI_CLK0M
3	GPIO_19	28	GND
4	GND	29	DSI_CLK0P
5	GPIO_17	30	CSI_D3M
6	CAM_HSYNC	31	CSI_D2P
7	I2C1_SDA_CSI0_DAT8	32	CSI_D3P
8	I2C1_SCL_CSI0_DAT9	33	CSI_D2M
9	CAM_D6	34	GND
10	CAM_D3	35	GND
11	CAM_D7	36	CSI_D1P
12	CAM_D5	37	CSI_CLK0M
13	CAM_D4	38	CSI_D1M
14	CAM_PCLK	39	CSI_CLK0P
15	CAM_D2	40	GND
16	GND	41	PCIE_RXP
17	CAM_nRST_CSI0_DAT10	42	CSI_D0M
18	CAM_VSYNC	43	PCIE_RXM
19	CAM_D1	44	CSI_D0P
20	CAM_D0	45	CLK1_P
21	GND	46	PCIE_TXP
22	CAM_SHDN_CSI0_DAT11	47	CLK1_N
23	DSI_D1M	48	PCIE_TXM
24	DSI_D0M	49	GND
25	DSI_D1P	50	GND

Table 16. J603 Header (Figure. 1. O)

Pin	Signal Name	Pin	Signal Name
1	GPIO_3	26	DSI_D1P
2	GPIO_8	27	GND
3	GND	28	DSI_CLK0M
4	GPIO_19	29	CSI_D3M
5	CAM_HSYNC	30	DSI_CLK0P
6	GPIO_17	31	CSI_D3P
7	I2C1_SCL_CSI0_DAT9	32	CSI_D2P
8	I2C1_SDA_CSI0_DAT8	33	GND
9	CAM_D3	34	CSI_D2M
10	CAM_D6	35	CSI_D1P
11	CAM_D5	36	GND
12	CAM_D7	37	CSI_D1M
13	CAM_PCLK	38	CSI_CLK0M
14	CAM_D4	39	GND
15	GND	40	CSI_CLK0P
16	CAM_D2	41	CSI_D0M
17	CAM_VSYNC	42	PCIE_RXP
18	CAM_nRST_CSI0_DAT10	43	CSI_D0P
19	CAM_D0	44	PCIE_RXM
20	CAM_D1	45	PCIE_TXP
21	CAM_SHDN_CSI0_DAT11	46	CLK1_P
22	GND	47	PCIE_TXM
23	DSI_D0M	48	CLK1_N
24	DSI_D1M	49	GND
25	DSI_D0P	50	GND

Table 17. JTAG Header (Figure. 1. P)

Pin	Signal Name
TP200	JTAG_TCK
TP201	JTAG_TMS
TP202	JTAG_TDI
TP203	JTAG_TDO
TP204	JTAG_TRSTB
TP205	JTAG_MOD
U114-PIN3	CPU_nRESET_Input
U114-PIN4	VDD_3P3V

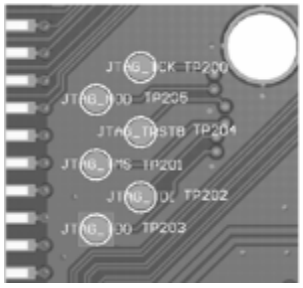


Table 18. J601 Header (Figure. 1. Q)

Pin	Signal Name	Pin	Signal Name
1	TRXP0	26	SD1_CLK
2	TRXP1	27	SD1_DAT0
3	TRXN0	28	SD1_DAT1
4	TRXN1	29	SD1_DAT2
5	GND	30	SD1_DAT3
6	GND	31	USB_5V
7	TRXP2	32	GND
8	TRXP3	33	USB_HUB_DM1
9	TRXN2	34	USB_HUB_DM2
10	TRXN3	35	USB_HUB_DP1
11	RGMII_LED_ACT	36	USB_HUB_DP2
12	RGMII_LED_1000	37	HPO_R
13	RGMII_LED_10_100	38	HP_nINSERT
14	EIM_D17	39	HPO_L
15	EIM_D18	40	HPO_GND
16	EIM_D19	41	MIC1_N
17	EIM_D16	42	MIC_GND
18	EIM_D28	43	LINEIN_R
19	EIM_D22	44	MIC_nDET_GPIO_16
20	EIM_A25	45	LINEIN_L
21	EIM_D20	46	LIN_GND
22	EIM_D21	47	SPK_LN
23	GND	48	SPK_LP
24	GND	49	SPK_RN
25	SD1_CMD	50	SPK_RP

3.2 Signal and Power Considerations

1. Each top and bottom of individual pins of the 50-pin expansion pin headers are connected to the same signals , please make sure to connect only one pin on one side when when design or connect to the daughter boards.
2. When providing power from the daughter board via the expansion pin headers, do not connect the 5V DC power input barrel on the mainboard at the same time.
3. The VCC_5V output current from the expansion headers output has a limit of 1A
4. The USB_5V output current from the USB headers has a limit of 1A
5. When providing power from the daughter board via the expansion pin headers, make sure to provide enough current (2A or more) to the mainboard
6. Speaker amplifier output is 1W

3.3 Boot Options

The board can be selected to boot up from on-board iNAND or micro-SD card. See Table 5 on page 8 for DIP switch settings.

3.4 GPIO Configuration Table

Pad	MUX MODE0							Sample Usage	
	ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0	HIO-PNL1280	HIO-POE1260
J601, J607									
EIM_A25		GPIO5_IO02				SPI4_SS1			
EIM_D16		GPIO3_IO16				SPI1_SCK		LCD_SPI_SCK	
EIM_D17	I2C3_SCL	GPIO3_IO17				SPI1_MISO		LCD_SPI_DO	
EIM_D18	I2C3_SDA	GPIO3_IO18				SPI1_MOSI		LCD_SPI_DI	
EIM_D19		GPIO3_IO19				SPI1_SS1		LCD_SPI_CS	
EIM_D20		GPIO3_IO20				SPI1_SS0			
EIM_D21	I2C1_SCL	GPIO3_IO21				SPI4_SCK			
EIM_D22		GPIO3_IO22				SPI4_MISO			
EIM_D24		GPIO3_IO24		SPI1_SS2	UART3_TXD	SPI4_SS2			
EIM_D25		GPIO3_IO25		SPI1_SS3	UART3_RXD	SPI4_SS3			
EIM_D28		GPIO3_IO28			SPI4_MOSI	I2C1_SDA			
GPIO_16	I2C3_SDA	GPIO7_IO11						MIC_Detect	
SD3_RST		GPIO7_IO08						Headphone_Detect	
J602,J608									
KEY_COL0		GPIO4_IO06	UART4_TXD		AUD5_TXC		SPI1_SCK		UART4_TXD
KEY_ROW0		GPIO4_IO07	UART4_RXD		AUD5_TXD		SPI1_MOSI		UART4_RXD
KEY_COL1		GPIO4_IO08	UART5_TXD		AUD5_TXFS		SPI1_MISO		UART5_TXD
KEY_ROW1		GPIO4_IO09	UART5_RXD		AUD5_RXD		SPI1_SS0		UART5_RXD
KEY_COL2		GPIO4_IO10			CAN1_TX		SPI1_SS1		
KEY_ROW2		GPIO4_IO11			CAN1_RX		SPI1_SS2		
KEY_COL3		GPIO4_IO12	I2C2_SCL						
KEY_ROW3		GPIO4_IO13	I2C2_SDA						
KEY_COL4		GPIO4_IO14	UART5_RTS				CAN2_TX		
KEY_ROW4		GPIO4_IO15	UART5_CTS				CAN2_RX		
GPIO_1		GPIO1_IO01	PWM2					TP_IRQ	
GPIO_3		GPIO1_IO03	CCM_CLKO2		I2C3_SCL			Camera_Clock	
GPIO_4		GPIO1_IO04						TP_Reset	
GPIO_5	I2C3_SCL	GPIO1_IO05						TP_I2C_SCL	
GPIO_6		GPIO1_IO06			I2C3_SDA			TP_I2C_SDA	
GPIO_7		GPIO1_IO07		CAN1_TX					
GPIO_9		GPIO1_IO09	PWM1					LCD_BLK_Ctl	
EIM_D24		GPIO3_IO24			UART3_TXD				UART3_TXD
EIM_D25		GPIO3_IO25			UART3_RXD				UART3_RXD
J603, J609									
GPIO_3		GPIO1_IO03	CCM_CLKO2		I2C3_SCL			CAM_MCLK	
GPIO_8		GPIO1_IO08		CAN1_RX				LCD_Power_Ctl	
GPIO_17		GPIO7_IO12						LCD_BLK_Power_Ctl	
GPIO_19		GPIO4_IO05						Camera I2C_SDA	
CSI0_DAT8		GPIO5_IO26	I2C1_SDA					Camera I2C_SCL	
CSI0_DAT9		GPIO5_IO27	I2C1_SCL						
CSI0_DAT10		GPIO5_IO28	UART1_TXD						UART1_TXD
CSI0_DAT11		GPIO5_IO29	UART1_RXD						UART1_RXD

4. Operating System

4.1 Host Operating System

a. Host OS:Ubuntu 12.04 64-bit
b. Host Build System: Yocto Embedded Linux

4.2 Target Operating System

a. Board u-boot version: based on Freescale u-boot-fslc-2014.01
b. Board kernel version: based on Freescale linux-imx-3.10.17
c. UI framework: Qt version 5.2.1
d. Embedded Linux Distribution: Poky 1.6.1
e. BSP: fsl-community-bsp-platform Daisy branch+ meta-hio + meta-qt5

4.3 U-boot Features

a. Based on Freescale Yocto u-boot-fslc-patches-2014.01
b. Support 3.5", 7", 10", 12" LCD panel option (models: SHARP LS035Y8DX02A, AUO A070STN01.1, AUO G101EVN01.0, AUO A116XW02V0,)
c. Support external USB drive image update via u-boot
d. Support micro-SD card image update via u-boot
e. Support HDMI display

4.4 Kernel Features

a. Based on Freescale linux-imx-3.10.17
b. Support HDMI and LCD dual display
c. Support analog speaker, line out and HDMI audio selection
d. USB to SATA support (Genesys Logic GL830)
e. Support CIFS
f. USB WiFi support (Realtek RTL8188EUS)

4.5 Rootfs filesystem Features

a. Based on Yocto core-image-minimal
b. Support minimal filesystem (hio-image-minimal)
c. Support minimal + qt5 filesystem (hio-image-fb)
d. Support x11 + sato + qt5 filesystem (hio-image-x11)

Refer to www.hioproject.org and https://github.com/HIO-Project for instructions of building the file systems.